Remarks/Arguments

The Office Action of June 20, 2003 and the references cited therein have been carefully studied and reviewed, and in view of the foregoing Amendment and following representations, reconsideration is respectfully requested.

1. The Rejection of Claim 11 Under 35 USC 103 As Being Unpatentable Over Bohr (USP 5,536,675) in View of Chang et al. (USP 6,326,310) and Wu (USP 6,165,854).

None of the references teach Applicants' claimed buffer layer.

Bohr (USP 5,536,675) discloses forming a trench oxide layer 252 corresponding at best to Applicants' claimed thermal oxide layer 114, followed by filling the trench with a first oxide layer (silicon dioxide). However, as admitted by the Examiner, Bohr fails to disclose the forming of any buffer layer just prior to the filling of the deep trench with the first oxide layer. That is, Bohr fails to disclose any step corresponding to Applicants claimed step (f), namely the forming of a buffer layer followed by a step (g) of filling the trench, **in which the buffer layer has been formed**, with an oxide layer. In particular, Bohr fails to disclose the forming of a buffer layer from one of a high temperature oxide layer, a middle temperature oxide layer and a plasma-enhanced oxide layer.

The reference to Chang et al. (USP 6,326,310) does not disclose a trench isolation structure comprising a buffer layer.

Wu also fails to teach a trench isolation structure comprising a buffer layer and, in particular, fails to teach a buffer layer comprising a high temperature oxide layer, a middle temperature oxide layer or a plasma-enhanced oxide layer.

Wu teaches a method forming a shallow trench isolation layer comprising the forming of a thermal oxide layer 10 along the walls defining the shallow trench (FIG. 4), and the filling of the shallow trench with an oxide layer 14 (FIG. 6). The thermal oxide layer 10 of Wu corresponds to the thermal oxide layer 252a of Bohr (FIG. 3B) and to the thermal oxide layer in Applicants' claimed step (d). The oxide layer 14 of Wu that fills the trench corresponds to the filler layer 260 of Bohr (FIG. 3E) and to the first oxide layer in Applicants' claimed step (g).

Wu does teach forming a layer 12 by PECVD between the thermal oxide layer 10 and the oxide filler layer 14. **However**, unlike Applicants' invention of claim 11, layer 12 of Wu is a silicon oxy**nitride** (SiON) layer, i.e., is not an **oxide** layer as set forth in Applicants' claimed step (f). Note, a nitride layer, such as the silicon oxynitride layer 12 of Wu, acts as a liner for the trench (col. 2, lines 14 – 25 and 56 – 63 of Wu), as distinguished from the high temperature oxide layer, middle temperature oxide layer or plasma-enhanced oxide layer that acts as a buffer layer in Applicants' invention.

Therefore, even assuming, *arguendo*, that one of ordinary skill in the art would have been motivated to have modified the method of Bohr by employing the SiON

layer 12 taught by Wu between the thermal oxide layer 252a and filler layer 260, the resulting method would still not meet Applicants' claim 11 as such a result would lack a step of forming a high temperature **oxide** layer, a middle temperature **oxide** layer or a plasma-enhanced **oxide** layer as a **buffer** layer. Accordingly, the references can not render obvious the subject matter of Applicants' claimed 11.

2. The Rejection of Claim 12 Under 35 USC 103 As Being Unpatentable Over Bohr (USP 5,536,675) in View of Chang et al. (USP 6,326,310) and Wu (USP 6,165,854).

None of the references teach Applicants' claimed use of the same sidewall spacer as a mask during a series of etching steps.

Applicants' Claim 12 sets forth steps of (1) etching a portion of a semiconductor substrate using a hard mask pattern 106, 108 and a sidewall spacer 110 as a mask to thereby form a shallow trench 112 (FIG. 9), (2) forming a thermal oxide layer 114 along inner walls of the semiconductor substrate that define opposed side walls and a bottom wall of the shallow trench (FIG. 10), and (3) etching the resulting structure using the hard mask pattern 106, 108 and the same sidewall spacer 110 used to form the shallow trench as a mask to extend the shallow trench deeper into the semiconductor substrate.

Bohr discloses a method in which a deep trench 242 (FIG. 3D) is formed by (1) etching a portion of a semiconductor substrate using a hard mask pattern 210, 220 and

a photoresist pattern 230 as a mask to thereby form a shallow trench 242a (FIG. 3A), (2) forming a thermal oxide layer 252a along inner walls of the semiconductor substrate that define opposed side walls and a bottom wall of the shallow trench (FIG. 3B), and (3) etching the resulting structure using a patterned photoresist layer 231 as a mask to extend the shallow trench deeper into the semiconductor substrate.

As admitted by the Examiner, Bohr fails to disclose the use of any sidewall spacer as an etching mask. More particularly, as distinguished from Applicants' method, as is now claimed, Bohr does not disclose or suggest the use a sidewall spacer in common to both form the shallow trench 242a, and to extend the shallow trench deeper after the thermal oxide layer 252 is formed.

Chang et al. teach a method of forming a "shallow" trench isolation using a series of sidewall spacers 208, 210 and 212, 214 formed one after another as etching masks to impart a desired profile , e.g., an inclined profile, to the "shallow" trench. Thus, Chang et al. also fails to teach using the same sidewall spacer as an etching mask in forming a first trench, such as that shown in FIG. 4B, and as a mask in a subsequent etching process used to extend the trench deeper.

The reference to Wu was relied on by the Examiner for the teachings therein associated with SiON layer 12, and thus does not overcome the deficiencies in the Bohr and Chang et al. references described above.

Therefore, none of the references teach a technique in which the same sidewall spacer is used to form a shallow trench in a first etching process, and then is also used to extend the shallow trench deeper in a second etching process. Accordingly, the references can not render obvious the subject matter of Applicants' claimed 11, particularly with respect to steps (c), (d) and (e) recited therein.

3. The Rejection of Claims 23 and 24 Under 35 USC 103 As Being Unpatentable Over Bohr (USP 5,536,675) in View of Chang et al. (USP 6,326,310) and Wu (USP 6,165,854).

Claims 23 and 24 each set forth a step removing the **entire** portion of the thermal oxide layer 114 (FIG. 10) that is disposed along the bottom of the shallow trench 112 to extend the shallow trench 112 deeper into the semiconductor substrate 102 and thereby **form a deep trench** 116 (FIG. 11) **that has substantially the same width as the shallow trench 112.**

Bohr fails to disclose such a step. In Bohr, **only a portion** of the oxide layer 252a lying along the bottom of the shallow trench 242a is removed, and the **deep trench** 242b (FIG. 3C) is formed to have **a width that is much smaller than that of the shallow trench 242a** (FIG. 3B).

Chang et al. also fails to disclose such a step. In fact, Chang et al. teaches away from Applicants' invention of claims 23 and 24. The entire purpose of the Chang et al.

method is to achieve a profiling wherein the deeper portions of the trench have widths that are significantly different from those of the shallower portions.

Again, Wu was merely relied on by the Examiner for the teachings therein associated with SiON layer 12, and thus does not overcome the deficiencies in the Bohr and Chang et al. references described above.

Therefore, the references can not render the subject matter of Applicant's claims 23 and 24 obvious under 35 USC 103 because the references do not suggest at least step (e) of the claims.

4. The Rejection of Claim 17 Under 35 USC 103 As Being Unpatentable Over Madan (USP 5,3350,941) in View of Wu (USP 6,165,854).

A. There is n motivation that would have motivated one of ordinary skill in the art to have combined the references

It is axiomatic that to establish a *prima facie* case of obviousness, based on a combination of references under 35 USC 103, the Examiner must identify suggestion that would have motivated one of ordinary skill in the art to have modified the references.

The Examiner finds that one of ordinary skill in the art would have been motivated to have modified the method of Madan to incorporate the silicon oxynitride layer 12 of Wu "in order to prevent parasitic leakage".

The Examiner has not established a *prima facie* case of obviousness because there is no suggestion that would have motivated one of ordinary skill in the art to have combined the references for the reason proposed by the Examiner.

Parasitic capacitance may occur as a so-called corner effect in trench isolation structures when the corner of the trench is sharp. Please refer to col. 2, lines 1 -10 of the Wu reference and, especially to USP 5, 521,422 referred to therein.

Madan discloses a trench isolation method in which bird's beak regions 26a, 26b, 28a, and 28b are formed at the sidewalls of trenches 34, 36 and 38 (FIG. 1e) to round the corners of the trenches. Hence, little, if any, parasitic leakage would occur at the corners. Any spurious leakage is prevented by the provision of channel stop regions 60.

Wu teaches another means of rounding the corners of the trenches. In the method taught by Wu, trenches 8 are formed using a hard mask pattern 4 (FIG. 3). The hard mask 4 is then removed to expose the substrate 2. Subsequently, the corners of the trenches 8 are rounded by depositing a layer of SiON 12 directly on the exposed substrate to thermally process the substrate 2 (col. 4, lines 7 – 14).

Applicants most strenuously assert that there is simply no suggestion from the references to add the SiON layer 12 of Wu to the structure disclosed by Madan after the trenches 34, 36 of Madan are formed as shown in FIG. 1e. As was previously mentioned, the corners of the substrate 10 of Madan have already been rounded by

the LOCOS structure 28 which, when etched, yields the resulting bird's beak regions 26b, 28a, and 28b. Therefore, adding the SiON layer would not serve "to prevent parasitic leakage". In other words, the methods disclosed by Madan and Wu would clearly be viewed by those of ordinary skill in the art as **alternative** techniques of rounding the corners of the substrates at the tops of the trenches to reduce parasitic capacitance. Accordingly, the rejection should be withdrawn.

B. None of the references teach Applicants' claimed buffer layer.

As discussed above in connection with the rejection of claim 11, layer 12 of Wu is a silicon oxynitride (SiON) layer, not an oxide layer as set forth in step (e) of Applicants' claim 17. The references to Madan and Wu can not render obvious the method of Applicants' claim 17 because neither of the references teach a step of forming a high temperature oxide layer, a middle temperature oxide layer or a plasma-enhanced oxide layer as a buffer layer in a shallow trench before the trench is filled with an oxide layer.

For these reasons, namely because of the lack of teachings in the references of the forming of a high temperature oxide layer, a middle temperature oxide layer or a plasma-enhanced oxide layer as a buffer layer in a shallow trench having a curvilinear interface at upper corners of the trench isolation region, it seen that the reference do not render Applicants' claims obvious under 35 USC 103. Accordingly, early reconsideration and allowance of the claims are respectfully requested.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, PLLC

By: Reg No 33289
for: Michael Stone
Reg. No. 32,442

ONE FREEDOM SQUARE
11951 FREEDOM DRIVE, SUITE 1260
RESTON VA 20190
Tel. (703) 715-0870
Fax (703) 715-0877

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